

**Low Complexity VLSI Architectures For LDPC
Decoders. By Daesun Oh**

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China science journal

A memory efficient partially parallel decoder architecture for quasi-cyclic LDPC codes [J]. IEEE Transactions on Very Large Scale Integration Daesun O and Parhi K

Citeulike: rdysydc's oh [2 articles]

by Daesun Oh, Keshab K. Parhi we propose low complexity implementations of sum-product algorithm (SPA) for decoding low-density parity-check (LDPC) codes.

Efficient multi-gb/s multi-mode ldpc decoder

This paper presents a novel multi-Gb/s multi-mode LDPC decoder architecture and efficient of very large-scale integration D. Oh, K. Parhi; Low-complexity

High-speed low- complexity architecture for

High-Speed Low-Complexity Architecture for Reed-Solomon codes, VLSI architectures: DOI: a high-speed, low-complexity VLSI architecture based on the

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Configurable m-factor vlsi dvb-s2 ldpc decoder

codes have improved Very Large Scale Integration Fanucci, Low complexity LDPC code decoders for D Oh, K Parhi, Min-sum decoder architectures with

A configurable and low complexity hard-decision

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IEEE Transactions on Very Large Scale Integration (VLSI) (LDPC) decoders. The proposed architecture leads to significant a novel low-complexity switch

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A VLSI Architecture and Low-Complexity Switch Network for Reconfigurable LDPC Decoders (Daesun Oh IEEE Transactions on Very Large Scale Integration

Low- complexity hierarchical mode decision

The low-complexity mode decision architecture proposed is thus a very good option for real mode decision for H.264/AVC and their respective VLSI architectures.

Flexible ldpc decoder architectures

Low complexity LDPC code decoders for next and X. Zeng, A flexible LDPC decoder architecture supporting two on Very Large Scale Integration

A flexible ldpc/turbo decoder architecture -

A Flexible LDPC/Turbo Decoder Architecture Yang Sun Low complexity LDPC code decoders for next IEEE Transactions on Very Large Scale Integration (VLSI

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Patent us8418023 - low density parity check

A method and system for decoding low density parity check (LDPC and low complexity comprising a low density parity check (LDPC) decoder in

A novel combinatorics-based reconfigurable bit

A Novel Combinatorics-Based Reconfigurable Bit Permutation Network and Its Circuit Implementation[J]. Chinese Journal of Electronics, 2015, 24(CJE-3):

Low-latency low- complexity channel decoder

low-complexity, low-error, First, a novel design methodology to design low-complexity VLSI architectures for non-binary LDPC decoders is presented.

Etri journal

His research interests include signal processing algorithms and SoC/VLSI low complexity hardware architecture low complexity at the realized LDPC decoder.

Dblp: ieee workshop on signal processing systems

Proceedings of the IEEE Workshop on Signal Processing Systems, in VLSI Architectures for Daesun Oh, Keshab K. Parhi: Low Complexity Implementations

Patent us8359522 - low density parity check

and they are more suitable for parallelization and low complexity a low density parity check (LDPC) decoder in architecture for regular

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This chapter provides first an overall survey of LDPC decoders, symbol-reliability-based message-passing decoding , low-complexity decoding for majority

Vlsi architectures for modern error-correcting

VLSI Architectures for Modern non-binary low-density parity-check (LDPC) theory of the codes and VLSI architecture design of their decoders,

The mathematics genealogy project - daesun oh

Daesun Oh . MathSciNet. Low Complexity VLSI Architectures for LDPC Decoders. Mathematics Subject Classification: 94 Information and communication, circuits .

Algorithms, complexity analysis and vlsi

Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation [Peter M. Kuhn] on Amazon.com. *FREE* shipping on qualifying offers. MPEG-4 is the

2008 42nd asilomar conference on signals, systems

Optimally quantized offset min-sum algorithm for flexible LDPC decoder (Daesun Oh low complexity decoder architecture for quasi-cyclic LDPC

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Efficient VLSI architectures for MIMO and cryptography It is of great interest to develop low-complexity and high-speed VLSI architectures for the MIMO

Low-power vlsi architectures for dct/dwt:

free approximations because they result in low power and low complexity error free VLSI architectures that provides high accuracy systems and

Patent us8656250 - low density parity check

A method and system for decoding low density parity check (LDPC and low complexity comprising a low density parity check (LDPC) decoder in

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